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Xyce™ Parallel Electronic Simulator Release Notes

Release 3.0.1

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Scope/Product Definition

The **Xyce** Parallel Electronic Simulator has been written to support, in a rigorous manner, the simulation needs of the Sandia National Laboratories electrical designers. Specific requirements include, among others, the ability to solve extremely large circuit problems by supporting large-scale parallel computing platforms, improved numerical performance and object-oriented code design and implementation.

The **Xyce** release notes describe:

- Hardware and software requirements
- New features and enhancements

- Any defects fixed since the last release
- Current known defects and defect workarounds

For up-to-date information not available at the time these notes were produced, please visit the **Xyce** web page at http://www.cs.sandia.gov/xyce.

Hardware/Software

This section gives basic information on supported platforms and hardware and software requirements for running **Xyce** 3.0.1

Supported Platforms

Xyce 3.0.1 currently supports any of the following operating system (all versions imply the earliest supported – **Xyce** generally works on later versions as well) platforms. These platforms are supported in the sense that they have been subject to certification testing for the **Xyce** version 3.0.1 release.

- SGI IRIX® 6.5.3, Workshop Compilers 7.4.2 (serial and parallel using SGI MPI)
- Redhat Linux®, Enterprise version 3 on Intel Pentium® architectures (serial and parallel using MPICH version 1.2.5.2 or LAM MPI version 7.0.6)
- Tru64 on HP/Compaq Alpha® (serial and parallel)
- FreeBSD on Intel Pentium® architectures (serial and parallel using MPICH or LAM MPI)
- Microsoft Windows® (serial)
- Apple® OS X (serial)

Build Capability but Not Supported

The platforms listed in this section are “not supported” in the sense that they are not subject to nightly regression testing, and they also were not subject to certification testing for the **Xyce** version 3.0.1 release. For large parallel platforms, such as ASCI White, this sort of testing is not a realistic option. These platforms are supported in the sense that **Xyce** 3.0.1 has been built for these platforms, and successfully executed on them. If a user needs to run **Xyce** 3.0.1 on one of these platforms, contact the **Xyce** team and we will work with you on a case-by-case basis.

- ASCI White (IBM) (parallel)

- Sandia Institutional Computational Clusters, ICC and NWCC (serial and parallel).
- **Xyce** 3.0.1 has not yet been ported to Thunderbird or RedStorm. However, these machines will be included for **Xyce** build support sometime during FY06.

Hardware Requirements

The following are estimated hardware requirements for running **Xyce**:

- 128MB memory recommended, 64 MB memory minimum – *memory requirements increase with circuit size*
- 50MB disk space (not including space needed for output files)

Software Requirements

Several libraries (all freely available from Sandia National Laboratories and other sites) are required to build **Xyce** on a platform. These are only required when building **Xyce** from source. These are:

- Trilinos Solver Library (Sandia, http://software.sandia.gov/Trilinos) . This is a suite of libraries including Amesos, KLU, AztecOO, Belos, Epetra, EpetraExt, Ifpack, NOX, LOCA, and y12m.
- SuperLU (http://www.nersc.org)
- Xyce Expression library (libexpr.a).
- BLAS (libblas.a).
- LAPack (liblapack.a).

For parallel builds, the following are additionally required:

- MPI (http://www-unix.mcs.anl.gov/mpi/) library for message passing (version 1.1 or higher), such as MPICH or LAM. The version used to build Xyce must be the same that is used for building Trilinos.
- Zoltan (Sandia, http://www.cs.sandia.gov/Zoltan) and its associated libraries (libzoltan.a, libzoltanCPP.a, libparmetis.a, libmetis.a)

Xyce Release 3.0.1 Documentation

The following **Xyce** documentation is available at the **Xyce** internal website in pdf form. Some of this documentation is in "Draft" mode and is incomplete.

- **Xyce** Users' Guide, Version 3.0.1
- **Xyce** Reference Guide, Version 3.0.1
- **Xyce** Release Notes, Version 3.0.1
- **Xyce** Theory Document
- **Xyce** Test Plan

New Features and Enhancements

This release is a minor release, fixing some issues that were found in Release 3.0 but containing no new major features. Highlights for this release include:

- Enhanced homotopy, including the ability to simultaneously use voltage limiting and homotopy algorithms.
- Additional roll-off parameter (NK) in BJT for improved PSPICE compatibility
- Improved error condition handling.
- Parser bug fixes.

For details of each of these new features, see the **Xyce** Users' Guide, and the **Xyce** Reference Guide.

Device Support

Table 1 contains a complete list of devices for **Xyce** Release 3.0.1. No new devices have been added in Release 3.0.1.

Device	Comments
Capacitor	Age-aware, semiconductor
Inductor	Nonlinear mutual inductor (see below)
Nonlinear Mutual Inductor	Sandia Core model (not fully PSpice compatible) Stability improvements.
Resistor	Semiconductor

Device	Comments
Diode (Level 1)	
Diode (Level 3)	Prompt photocurrent radiation model
Diode (Level 4)	Generic photocurrent source model
Independent Voltage Source (VSRC)	
Independent Current Source (ISRC)	
Voltage Controlled Voltage Source (VCVS)	
Voltage Controlled Current Source (VCCS)	
Current Controlled Voltage Source (CCVS)	
Voltage Controlled Current Source (CCCS)	
Nonlinear Dependent Source (B Source)	
Bipolar Junction Transistor (BJT) (Level 1)	
Bipolar Junction Transistor (BJT) (Level 2)	Prompt photocurrent radiation model.
Bipolar Junction Transistor (BJT) (Level 3)	Neutron-effects model.
Bipolar Junction Transistor (BJT) (Level 4)	Prompt photocurrent radiation model (same as level 2).
Junction Field Effect Transistor (JFET) (Level 1)	SPICE-compatible JFET model.
Junction Field Effect Transistor (JFET) (Level 2)	Shockley JFET model.
MESFET	
MOSFET (Level 1)	
MOSFET (Level 3)	
MOSFET (Level 9)	BSIM3 model. Initial condition support.
MOSFET (Level 10)	BSIM SOI model with initial condition support.
MOSFET (Level 18)	VDMOS model.
MOSFET (Level 19)	VDMOS photocurrent model.
Transmission Line	Lossless.
Controlled Switch (S,W) (VSWITCH/ISWITCH)	Voltage or current controlled.
Generic Switch (SW)	Controlled by an expression.

Device	Comments
PDE Devices (Level 1)	one-dimensional
PDE Devices (Level 2)	two-dimensional

Table 1: Devices Supported by Xyce.

Robustness Improvements

- Improvement of homotopy algorithms for large MOSFET circuits, including SOI circuits.

Defects of Release 3.0 Fixed in this Release

Defect	Description
Duplicate-name checker incorrectly handles Y devices. [Bug 803]	Checking of Y device names now includes both fields necessary for unique device naming.
Output columns merge together. [Bug 790]	Output manager has been changed to assure that output columns are always separated by spaces even when the numbers get very large.
Incorrect transition from DCOP to Transient when homotopy used. [Bug 834]	This has been fixed, and homotopy runs now enter the transient phase correctly.
Homotopy requires voltlim to be turned off. [Bug 822]	Code has been changed so that voltlim is no longer incompatible with homotopy.

Table 2: Fixed Defects.

Known Defects and Workarounds

Defect	Description
BSIM SOI default parameters not correct [Bug 879]	The default values for the parameters TOX, CLC, CLE, KETA, BETA0 and DELVT are not correct in Xyce 3.0.1. Additionally, the parameters CGSO and CGDO are not computed correctly from input parameters even if the correct value of TOX is specified. This will be fixed shortly in an "emergency patch release" version 3.0.2. *Workaround:* Specify the correct default values for all of these parameters in any BSIM SOI model cards you use. The default values are: TOX=100e-10, CLC=1e-8, CLE=0.0, KETA=-0.6, BETA0=0.0, DELVT=0.0. CGSO and CGDO are computed from several other model parameters. If DLC is not specified, the value of CGSO is given by $\texttt{CGSO} = 0.6 * \texttt{XJ} * (3.453133e-11)/\texttt{TOX}$. If DLC is given, CGSO is given by $\texttt{CGSO} = \texttt{DLC} * (3.453133e-11)/\texttt{TOX} - \texttt{CGSL}$. Similarly, CGDO is given by $\texttt{CGDO} = 0.6 * \texttt{XJ} * (3.453133e-11)/\texttt{TOX}$ if DLC is not set and by $\texttt{CGDO} = \texttt{DLC} * (3.453133e-11)/\texttt{TOX} - \texttt{CGDL}$ if DLC is set.
.DC sweep output.	.DC sweep calculation does not automatically output sweep results. *Workaround:* Use .PRINT statement to output sweep variable results.
Failure for netlists using ChileSPICE digital primitives.	**Xyce** does not currently support the use of digital primitives.
BJT Current Crowding	"Timestep too small" failures can result when IRB nonzero with level 2 and level 4 BJT *Workaround:* If such failure observed, disable current crowding effect by setting IRB to zero in all BJT models. Please feed back such circuits to the **Xyce** development team so that this bug can be characterized and eliminated.
Microsoft Windows installation restrictions	Users with insufficient privileges (i.e. Limited Account) are not permitted to install **Xyce** into folders on the System Drive (usually C:). *Workaround:* First, manually create the desired folder on the System Drive. It is then possible to install **Xyce** into this folder by following the standard Setup procedure.

Defect	Description
Xyce installer for Windows fails when Cygwin already installed [Bug 835]	The Xyce installer for Windows assumes that there is no existing Cygwin installation on the user's computer and attempts to use a small subset of Cygwin utilities included with it. If Cygwin is already installed, the batch file will exit with an uninformative error. *Workaround:* There is a way to install Xyce by adapting the script to use the pre-installed Cygwin utilities. Please contact the Xyce development team for specific instructions and assistance until we have adapted the installer for the case where Cygwin is already installed.
MPICH parallel runs may not exit cleanly	**Xyce** may not exit cleanly if it encounters certain errors during parsing. *Workaround:* If **Xyce** appears to hang, manually terminate each process. Usually a `SIGTERM` or `^C` is sufficient to halt the job. Users running on the Alpha should manually check for zombie processes after **Xyce** error exits, and kill them if necessary.
Incompatible proprietary file formats.	Netlists created with programs like Microsoft Word and Microsoft Wordpad will not run in **Xyce**. **Xyce** does not recognize proprietary file formats. *Workaround:* It is best not to use such programs to create netlists, unless netlists are saved as *.txt files. If you must use a Microsoft editor, it is better to use Microsoft Notepad. In general, the best solution is to use a Unix-style editor, such as Vi, Gvim, or Emacs.
Expressions in the `.PRINT` line can't use variables specified by `.PARAM` statements.	Specifying expressions in the `.PRINT` line is a new **Xyce** capability. It is very useful, but is unable to use `.PARAM` variables. *Workaround:* For now, the only solution is to not use `.PARAM` variables in `.PRINT` statement expressions. This will be fixed for a later release.
One known instance of restart results not matching original run results.	There is one case for a customer's parallel run of a large digital circuit of BSIM3's where the restart output does not match the original results for the same time range. *Workaround:* The only choice for now is to check the restart results against the baseline results for some block if the run results have a very tight tolerance for success. It is suggested to overlap the original run time with the restart time allowing comparison.
Duplicate node names in `.SUBCKT` [bug 784]	Duplicate node names in a `.SUBCKT` specification will lead to incorrect results. Users must take care that all nodes specified on a `.SUBCKT` line are unique in Xyce 3.0.1.

Defect	Description
Lead currents in B/E/F/G/H source and switch expressions [bug 801]	Use of lead currents in B/E/F/G/H source and switch expressions will lead to incorrect results. A fatal diagnostic should be generated for such usage, but is not. The only supported use of lead currents in **Xyce**3.0.1 is on `.PRINT` lines.

Table 3: Known Defects and Workarounds.

Incompatibilities With Other Circuit Simulators

Issue	Comment
.SAVE does not work.	**Xyce** does not support this. Use .PRINT instead.
.OP is not complete	A .OP netlist will run in **Xyce**, but will not produce the extra output normally associated with the .OP statement.
Pulsed source rise time of zero.	A requested pulsed source rise/fall time of zero really is zero in Xyce. In other simulators, requesting a zero rise/fall time causes them to use the printing interval found on the .TRAN line.
Mutual Inductor Model.	Not the same as PSpice. This is a Sandia developed model but is compatible with Cadence PSpice parameter set.
.PRINT line shorthand.	Output variables have to be specified as V(node) or I(source). Specifying the node alone will not work. Also, specifying V(*) or I(*) (to get all voltages or currents) will not work.
BSIM3 level.	In **Xyce** the BSIM3 level=9. Other simulators have different levels for the BSIM3.
BSIM SOI v3.2 level.	In **Xyce** the BSIM SOI (v3.2) level=10. Other simulators have different levels for the BSIM SOI.
Node names vs. device names.	Currently, circuit nodes and devices MUST have different names in **Xyce**. Some simulators can handle a device and a node with the same name, but **Xyce** cannot.
Interactive mode.	**Xyce** does not have an interactive mode.
ChileSPICE-specific ”operating point voltage sources.”	These are not currently supported within **Xyce**. *However...* **Xyce** does support ”IC=<value>” statements for capacitors, inductors, and the two BSIM devices which will automatically set these voltage drops at the beginning of a transient simulation.
Syntax for .STEP is different.	The manner of specifying a model parameter to be swept is slightly different. Also, it is not possible to do a .STEP sweep over a global parameter. See the Users' and Reference Guides for details.

Table 4: Incompatibilities with other circuit simulators.

Important Changes to **Xyce** Usage Since the Last Release.

Table 5 lists some usage changes for **Xyce**.

Issue	Comment
The TCAD/PDE devices no longer use the letter “Z” as their identifier in the nelist.	This has been changed to “YPDE”. This was done to allow for the MESFET to use the letter “Z”, to maintain compatibility with SPICE. [Bug 655]

Table 5: Changes to netlist specification since the last release.

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Trademarks

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